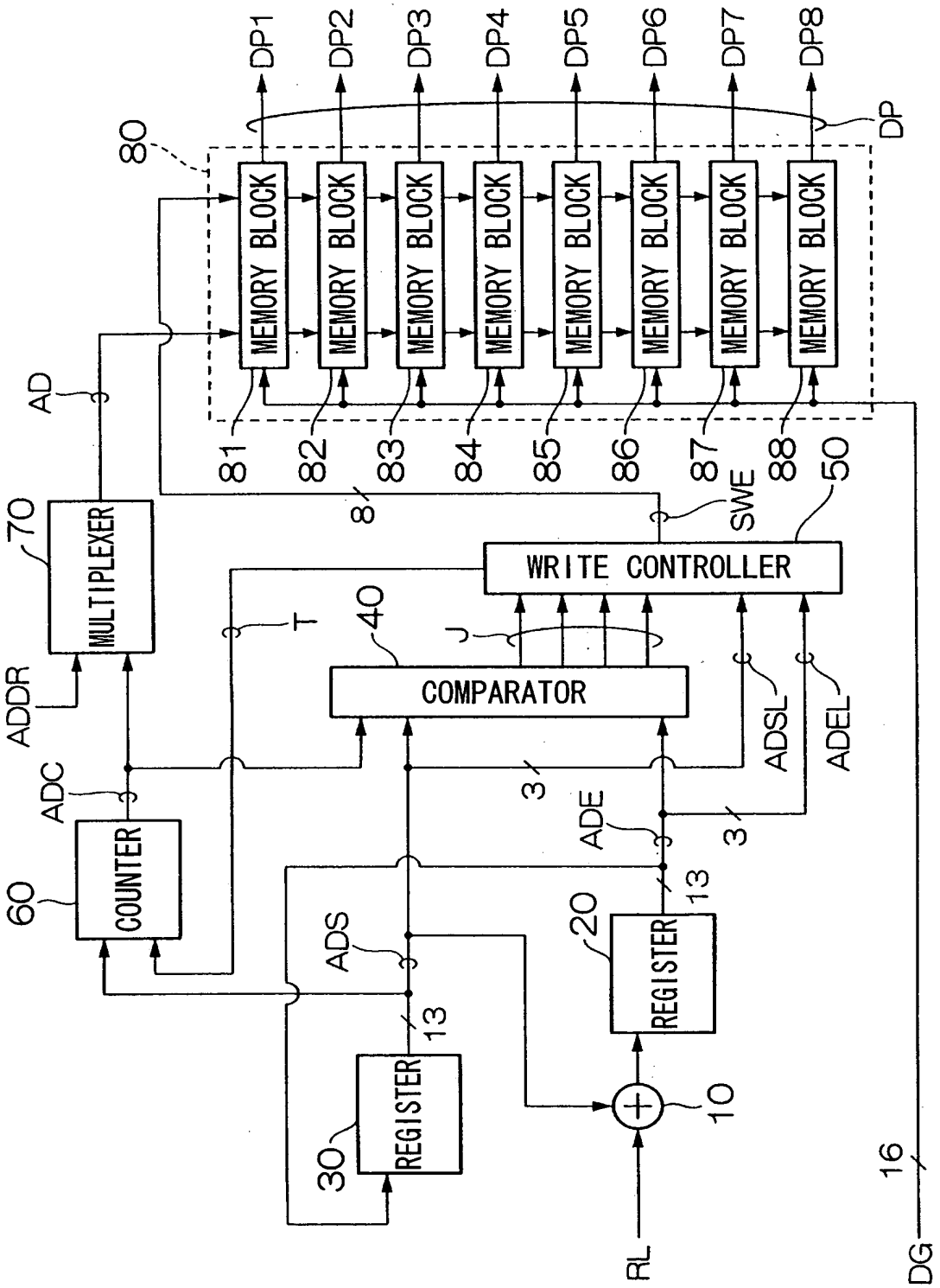
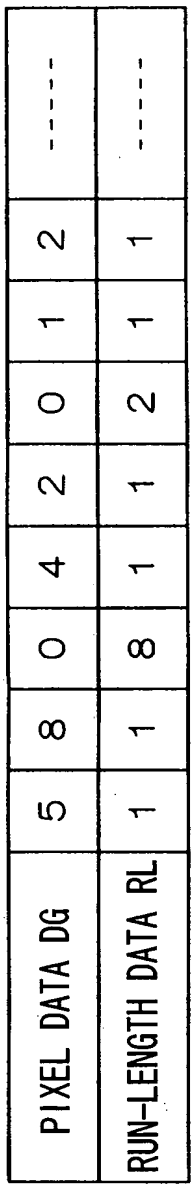
FIG. 1


DP1
DP2
DP3
DP4
DP5
DP6
DP7
DP8
DP
80
MEMORY BLOCK
AD
81
82
83
84
85
86
87
88
50
SWE
WRITE CONTROLLER
70
MULTIPLEXER
T
40
J
COMPARATOR
ADDR
ADC
ADSL
ADEL
3
ADE
60
COUNTER
ADS
13
20
REGISTER
30
REGISTER
10
RL
16
DG



PIXEL DATA DG	5	8	0	4	2	0	1	2	-----
RUN-LENGTH DATA RL	1	1	8	1	1	2	1	1	-----

FIG. 2A

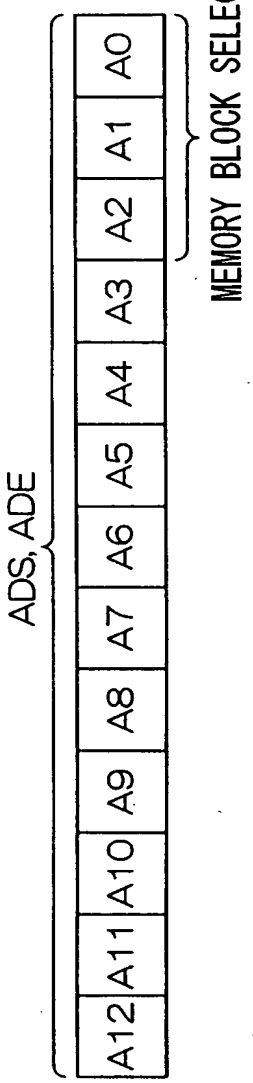


FIG. 2B

FIG. 3

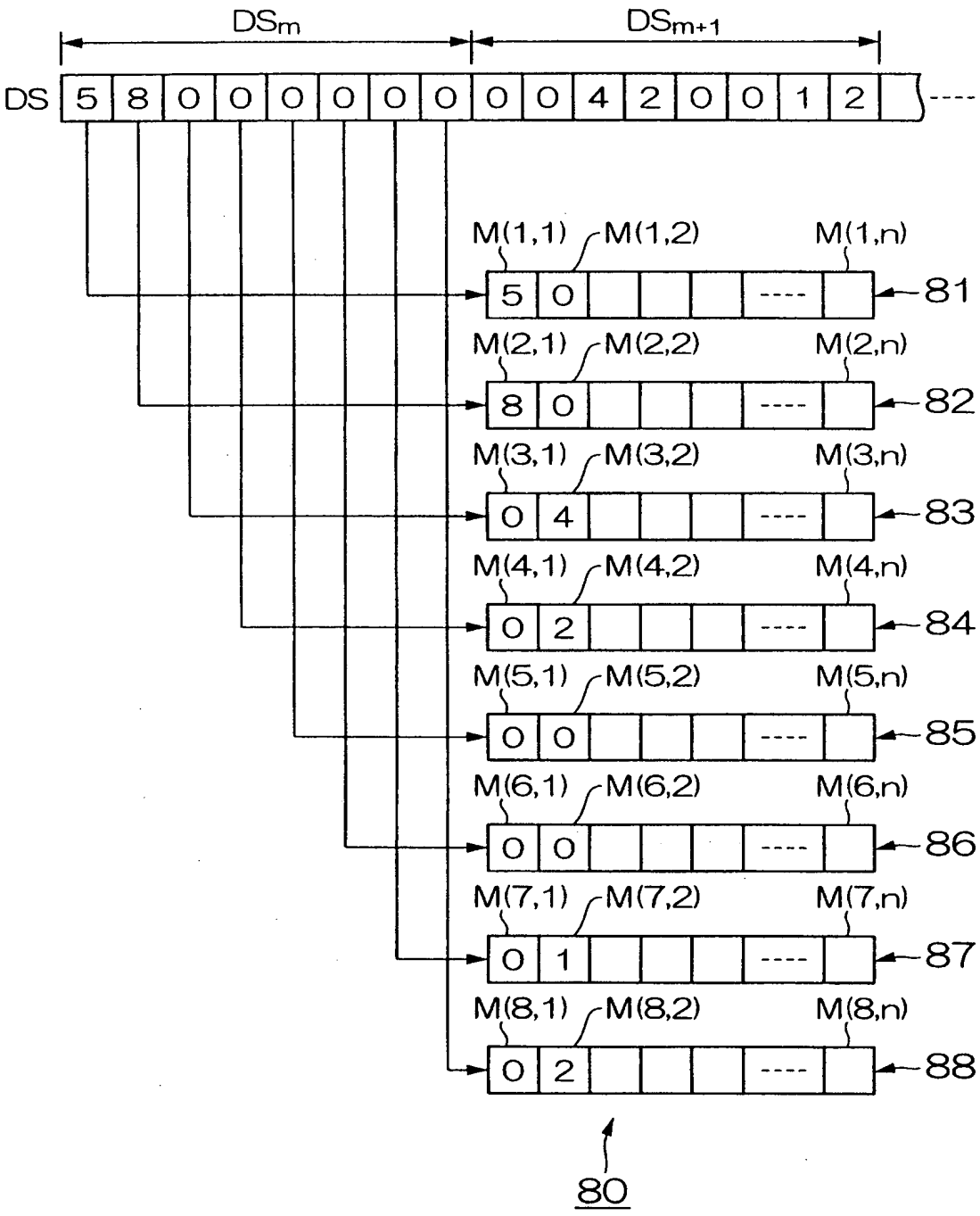

DSm
DSm+1
DS
5 8 0 0 0 0 0 0 0 0 4 2 0 0 1 2
M(1,1) M(1,2) M(1,n)
5 0 ---- 81
M(2,1) M(2,2) M(2,n)
8 0 ---- 82
M(3,1) M(3,2) M(3,n)
0 4 ---- 83
M(4,1) M(4,2) M(4,n)
0 2 ---- 84
M(5,1) M(5,2) M(5,n)
0 0 ---- 85
M(6,1) M(6,2) M(6,n)
0 0 ---- 86
M(7,1) M(7,2) M(7,n)
0 1 ---- 87
M(8,1) M(8,2) M(8,n)
0 2 ---- 88
80

FIG. 4A

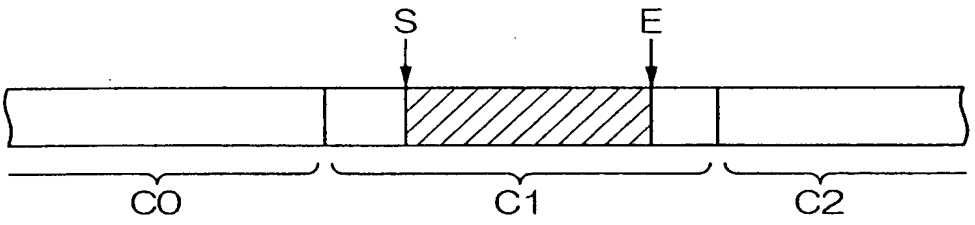


FIG. 4B

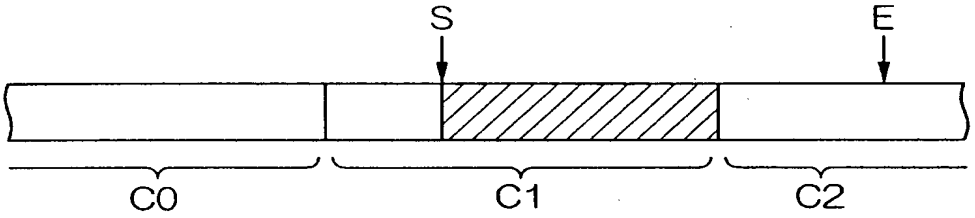


FIG. 4C

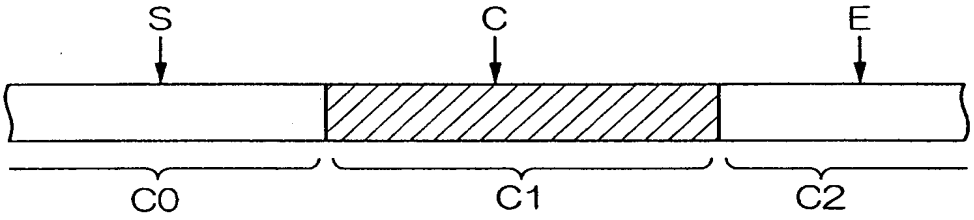
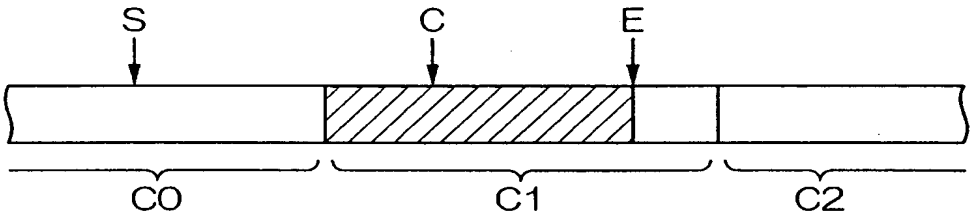



FIG. 4D